UNITRODE

UC2909
UC3909

Switchmode Lead-Acid Battery Charger

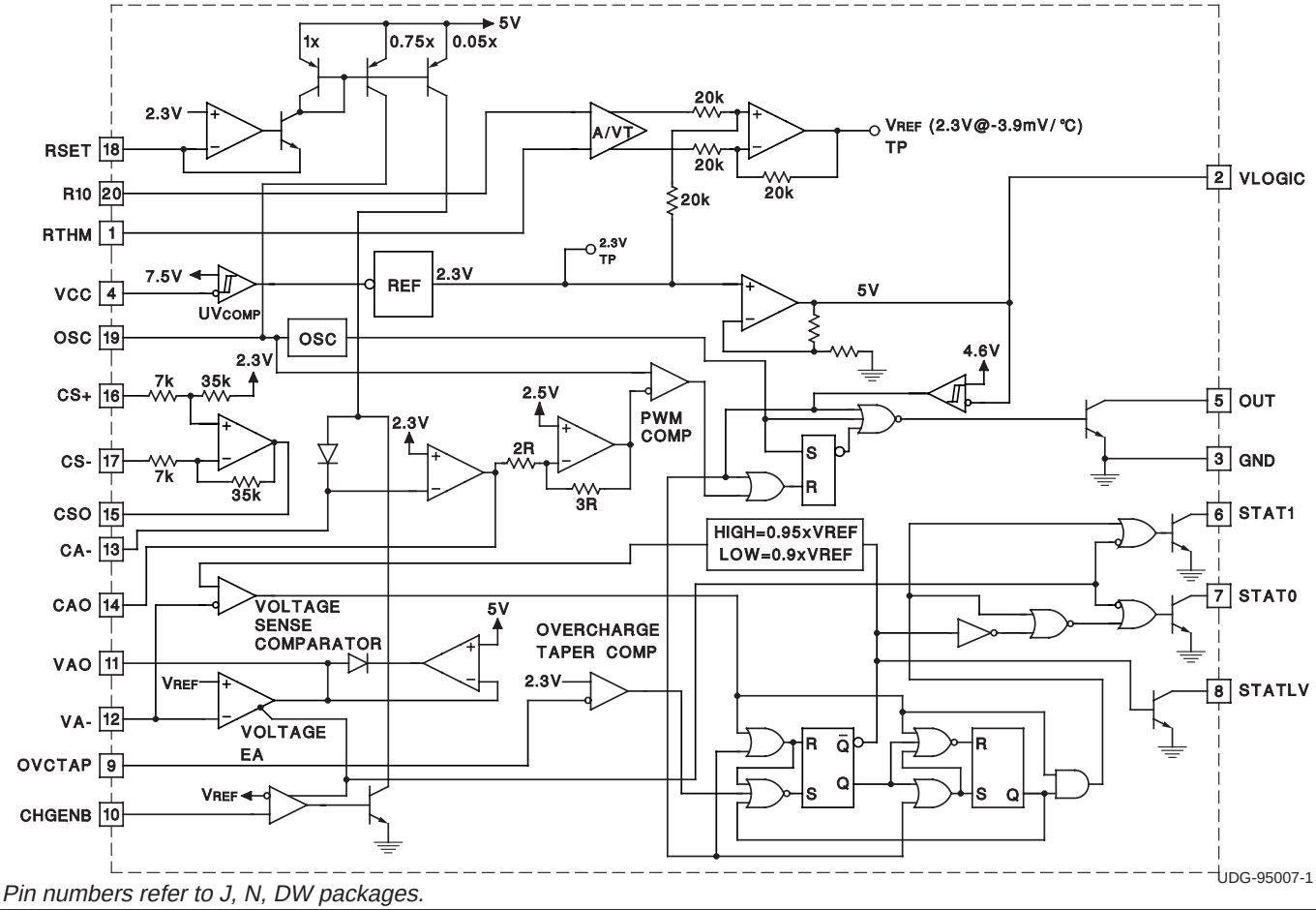
FEATURES

- Accurate and Efficient Control of Battery Charging
- Average Current Mode Control from Trickle to Overcharge
- Resistor Programmable Charge Currents
- Thermistor Interface Tracks Battery Requirements Over Temperature
- Output Status Bits Report on Four Internal Charge States
- Undervoltage Lockout Monitors VCC and VREF

DESCRIPTION

The UC3909 family of Switchmode Lead-Acid Battery Chargers accurately controls lead acid battery charging with a highly efficient average current mode control loop. This chip combines charge state logic with average current PWM control circuitry. Charge state logic commands current or voltage control depending on the charge state. The chip includes undervoltage lockout circuitry to insure sufficient supply voltage is present before output switching starts. Additional circuit blocks include a differential current sense amplifier, a 1.5% voltage reference, a –3.9mV/°C thermistor linearization circuit, voltage and current error amplifiers, a PWM oscillator, a PWM comparator, a PWM latch, charge state decode bits, and a 100mA open collector output driver.

BLOCK DIAGRAM



UDG-95007-1

Pin numbers refer to J, N, DW packages.

ABSOLUTE MAXIMUM RATINGS

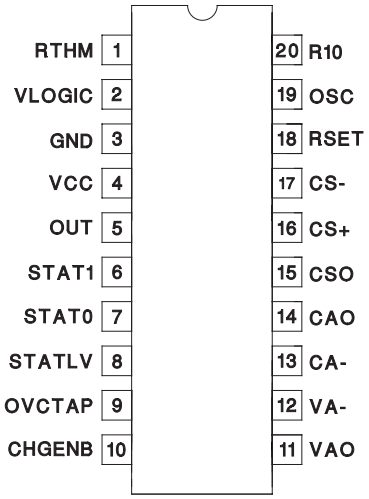
Supply Voltage (VCC), OUT, STAT0, STAT1 . . . . . 40V
Output Current Sink 0.1A
CS+, CS- . . . . . -0.4 to VCC (Note 1)
Remaining Pin Voltages. . . . . -0.3V to 9V
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

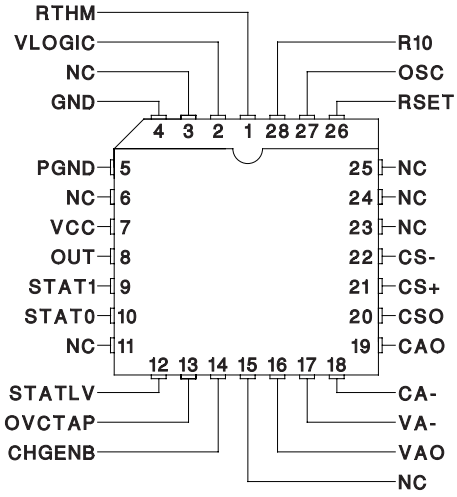
Note 1: *Voltages more negative than -0.4V can be tolerated if current is limited to 50mA.*

CONNECTION DIAGRAMS

DIL-20, (Top View)
J or N, DW Packages



LCC-28, PLCC-28 (Top View)
L, Q Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –40°C to +85°C for UC2909; °0C to +70°C for UC3909; C_T = 330pF, R_{SET} = 11.5k, R10 = 10k, R_{THM} = 10k, V_{CC} = 15V, Output no load, R_{STAT0} = R_{STAT1} = 10k, CHGENB = OVCTAP = VLOGIC, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense AMP (CSA) Section	V_{ID} = CS+ – CS–				
DC Gain	CS– = 0, CS+ = -50mV; CS+ = –250mV	4.90	5	5.10	V/V
	CS+ = 0, CS– = 50mV; CS–- = 250mV	4.90	5	5.10	V/V
V_{OFFSET} (V_{CSO} – V_{CAO})	CS+ = CS– = 2.3V, CAO = CA–			15	mV
CMRR	V_{CM} = –0.25 to VCC – 2, 8.8 < VCC < 14	50			dB
	V_{CM} = –0.25 to VCC, 14 < VCC < 35	50			dB
V_{OL}	V_{ID} = –550mV, –0.25V < VCM < VCC–2, I_O = 500µA		0.3	0.6	V
V_{OH}	V_{ID} = +700mV, –0.25V < VCM < VCC–2, I_O = –250µA	5.2	5.7	6.2	V
Output Source Current	V_{ID} = +700mV, CSO = 4V		–1	–0.5	mA
Output Sink Current	V_{ID} = –550mV, CSO = 1V	3	4.5		mA
3dB Bandwidth	V_{ID} = 90mV, V_{CM} = 0V	200			kHz

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Error Amplifier (CEA) Section					
I_B	8.8V < VCC < 35V, V_{CHGENB} = V_{LOGIC}		0.1	0.8	µA
V_{IO} (Note 2)	8.8V < VCC < 35V, CAO = CA–			10	mV
A_{VO}	1V < VAO < 4V	60	90		dB
GBW	T_J = 25°C, F = 100kHz	1	1.5		MHz
V_{OL}	I_O = 250µA		0.4	0.6	V
V_{OH}	I_O = –5mA	4.5	5		V
Output Source Current	CAO = 4V		–25	–12	mA
Output Sink Current	CAO = 1V	2	3		mA
I_{CA}–, $I_{TRCK_CONTROL}$	V_{CHGENB} = GND	8.5	10	11.5	µA
Voltage Amplifier (CEA) Section					
I_B	Total Bias Current; Regulating Level		0.1	1	µA
V_{IO} (Note 2)	8.8V < VCC < 35V, VCM = 2.3V, VAO = VA–		1.2		mV
A_{VO}	1V < CAO < 4V	60	90		dB
GBW	T_J = 25°C, F = 100kHz	0.25	0.5		MHz
V_{OL}	I_O = 500µA		0.4	0.6	V
V_{OH}	I_O = –500µA	4.75	5	5.25	V
Output Source Current	CAO = 4V	–2	–1		mA
Output Sink Current	CAO = 1V	2	2.5		mA
VAO Leakage: High Impedance State	V_{CHGENB} = GND, STAT0 = 0 & STAT1 = 0, VAO = 2.3V	–1		1	µA
Pulse Width Modulator Section					
Maximum Duty Cycle	CAO = 0.6V	90	95	100	%
Modulator Gain	CAO = 2.5V, 3.2V	63	71	80	%/V
OSC Peak			3		V
OSC Valley			1		V
Oscillator Section					
Frequency	8.8V < VCC < 35V	198	220	242	kHz
Thermistor Derived Reference Section	V_{ID} = V_{RTHM} – V_{R10}				
Initial Accuracy, VAO (RTHM = 10k)	V_{ID} = 0, R10 = RTHM =10k (Note 3)	2.2655	2.3	2.3345	V
	V_{ID} = 0, R10 = RTHM =10k, –40°C ≤T_A < 0°C (Note 3)	2.254	2.3	2.346	V
Line Regulation	V_{CC} = 8.8V to 35V		3	10	mV
VAO	RTHM = 138k, R10 = 10k	2.458	2.495	2.532	V
	RTHM = 138k, R10 = 10k, -40°C ≤ T_A < 0°C	2.445	2.495	2.545	V
	RTHM = 33.63k, R10 = 10k	2.362	2.398	2.434	V
	RTHM = 33.63k, R10 = 10k, -40°C ≤ T_A < 0°C	2.350	2.398	2.446	V
	RTHM = 1.014k, R10 = 10k	2.035	2.066	2.097	V
	RTHM = 1.014k, R10 = 10k, -40°C ≤ T_A < 0°C	2.025	2.066	2.107	V
Charge Enable Comparator Section (CEC)					
Threshold Voltage	As a function of VA–	0.99	1	1.01	V/V
Input Bias Current	CHGENB = 2.3V	–0.5	–0.1		µA

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Sense Comparator Section (VSC)					
Threshold Voltage	STAT0 = 0, STAT1 = 0, Function of V_{REF}	0.945	0.95	0.955	V/V
	STAT0 = 1, STAT1 = 0, Function of V_{REF}	0.895	0.9	0.905	V/V
Over Charge Taper Current Comparator Section (OCTIC)					
Threshold Voltage	Function of 2.3V REF, CA- = CAO	0.99	1	1.01	V/V
Input Bias Current	OVCTAP = 2.3V	–0.5	–0.1		µA
Logic 5V Reference Section (VLOGIC)					
VLOGIC	VCC = 15V	4.875	5.0	5.125	V
Line Regulation	8.8V < V_{CC} < 35V		3	15	mV
Load Regulation	0 < I_O < 10mA		3	15	mV
Reference Comparator Turn-on Threshold			4.3	4.8	V
Short Circuit Current	V_{REF} = 0V	30	50	80	mA
Output Stage Section					
I_{SINK} Continuous			50		mA
I_{PEAK}			100		mA
V_{OL}	I_O=50mA		1	1.3	V
Leakage Current	V_{OUT}=35V			25	µA
STAT0 & STAT1 Open Collector Outputs Section					
Maximum Sink Current	V_{OUT} = 8.8V	6	10		mA
Saturation Voltage	I_{OUT} = 5mA		0.1	0.45	V
Leakage Current	V_{OUT} = 35V			25	µA
STATLV Open Collector Outputs Section					
Maximum Sink Current	V_{OUT} = 5V	2.5	5		mA
Saturation Voltage	I_{OUT} = 2mA		0.1	0.45	V
Leakage current	V_{OUT} = 5V			3	µA
UVLO Section					
Turn-on Threshold		6.8	7.8	8.8	V
Hysteresis		100	300	500	mV
I_{CC} Section					
I_{CC} (run)	(See Fig. 1)		13	19	mA
I_{CC} (off)	VCC = 6.5V		2		mA

***Note 2**: VIO is measured prior to packaging with internal probe pad.*
***Note 3**: Thermistor initial accuracy is measured and trimmed with respect to VAO; VAO = VA–.*

PIN DESCRIPTIONS

CA–: The inverting input to the current error amplifier.

CAO: The output of the current error amplifier which is internally clamped to approximately 4V. It is internally connected to the inverting input of the PWM comparator.

CS–, CS+: The inverting and non-inverting inputs to the current sense amplifier. This amplifier has a fixed gain of five and a common-mode voltage range of from –250mV to +VCC.

CSO: The output of the current sense amplifier which is internally clamped to approximately 5.7V.

CHGENB: The input to a comparator that detects when battery voltage is low and places the charger in a trickle charge state. The charge enable comparator makes the output of the voltage error amplifier a high impedance while forcing a fixed 10µA into CA– to set the trickle charge current.

PIN DESCRIPTIONS (cont.)

GND: The reference point for the internal reference, all thresholds, and the return for the remainder of the device. The output sink transistor is wired directly to this pin.

OVCTAP: The overcharge current taper pin detects when the output current has tapered to the float threshold in the overcharge state.

OSC: The oscillator ramp pin which has a capacitor (C_T) to ground. The ramp oscillates between approximately 1.0V to 3.0V and the frequency is approximated by:

$$frequency = \frac{1}{1.2 \bullet C_T \bullet R_{SET}}$$

OUT: The output of the PWM driver which consists of an open collector output transistor with 100mA sink capability.

R10: Input used to establish a differential voltage corresponding to the temperature of the thermistor. Connect a 10k resistor to ground from this point.

RSET: A resistor to ground programs the oscillator charge current and the trickle control current for the oscillator ramp.

The oscillator charge current is approximately $\frac{1.75}{R_{SET}}$.

The trickle control current ($I_{TRCK_CONTROL}$) is approximately $\frac{0115}{R_{SET}}$.

RTHM: A 10k thermistor is connected to ground and is thermally connected to the battery. The resistance will vary exponentially over temperature and its change is used to vary the internal 2.3V reference by –3.9mV/°C. The recommended thermistor for this function is part number L1005-5744-103-D1, Keystone Carbon Company, St. Marys, PA.

STAT0: This open collector pin is the first decode bit used to decode the charge states.

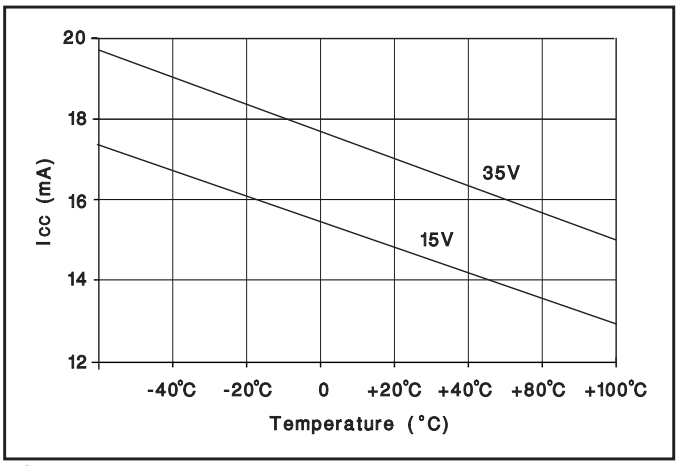


Figure 1. I_{CC} vs. temperature.

STAT1: This open collector pin is the second decode bit used to decode the charge states.

STATLV: This bit is high when the charger is in the float state.

VA–: The inverting input to the voltage error amplifier.

VAO: The output of the voltage error amplifier. The upper output clamp voltage of this amplifier is 5V.

VCC: The input voltage to the chip. The chip is operational between 7.5V and 40V and should be bypassed with a 1µF capacitor. A typical I_{CC} vs. temperature is shown in Figure 1.

VLOGIC: The precision reference voltage. It should be bypassed with a 0.1µF capacitor.

Charge State Decode Chart

STAT0 and STAT1 are open collector outputs. The output is approximately 0.2V for a logic 0.

	STAT1	STAT0
Trickle Charge	0	0
Bulk Charge	0	1
Over Charge	1	0
Float Charge	1	1

APPLICATION INFORMATION

A Block Diagram of the UC3909 is shown on the first page, while a Typical Application Circuit is shown in Figure 2. The circuit in Figure 2 requires a DC input voltage between 12V and 40V.

The UC3909 uses a voltage control loop with average current limiting to precisely control the charge rate of a lead-acid battery. The small increase in complexity of average current limiting is offset by the relative simplicity of the control loop design.

CONTROL LOOP

Current Sense Amplifier

This amplifier measures the voltage across the sense resistor RS with a fixed gain of five and an offset voltage of 2.3V. This voltage is proportional to the battery current. The most positive voltage end of RS is connected to CS- ensuring the correct polarity going into the PWM comparator.

CSO = 2.3V when there is zero battery current.

RS is chosen by dividing 350mV by the maximum allowable load current. A smaller value for RS can be chosen to reduce power dissipation.

Maximum Charge Current, Ibulk, is set by knowing the maximum voltage error amplifier output, V_{OH} = 5V, the maximum allowable drop across RS, and setting the resistors RG1 and RG2 such that;

$$\frac{RG1}{RG2} = \frac{5 \bullet V_{RS}}{VLOGIC - CA-} = \frac{5 \bullet V_{RS}}{5V - 2.3V} = \frac{5 \bullet V_{RS}}{2.7V} = 1.852 \bullet I_{BULK} \bullet RS \quad (1)$$

The maximum allowable drop across RS is specified to limit the maximum swing at CSO to approximately 2.0V to keep the CSO amplifier output from saturating.

No charge/load current: V_{CSO} = 2.3V,

Max charge/load current: $V_{max(CSO)}$ = 2.3V–2.0V = 0.3V

Voltage Error Amplifier:

The voltage error amplifier (VEA) senses the battery

voltage and compares it to the 2.3V – 3.9mV/°C thermistor generated reference. Its output becomes the current command signal and is summed with the current sense amplifier output. A 5.0V voltage error amplifier upper clamp limits maximum load current. During the trickle charge state, the voltage amplifier output is opened (high impedance output) by the charge enable comparator. A trickle bias current is summed into the CA– input which sets the maximum trickle charge current.

The VEA, V_{OH} = 5V clamp saturates the voltage loop and consequently limits the charge current as stated in Equation 1.

During the trickle bias state the maximum allowable charge current (ITC) is similarly determined:

$$ITC = \frac{I_{TRICK_CONTROL} \bullet RG1}{RS \bullet 5} \quad (2)$$

$I_{TRCK_CONTROL}$ is the fixed control current into CA–. $I_{TRCK_CONTROL}$ is 10µA when R_{SET} = 11.5k. See RSET pin description for equation.

Current Error Amplifier

The current error amplifier (CA) compares the output of the current sense amplifier to the output of the voltage error amplifier. The output of the CA forces a PWM duty cycle which results in the correct average battery current. With integral compensation, the CA will have a very high DC current gain, resulting in effectively no average DC current error. For stability purposes, the high frequency gain of the CA must be designed such that the magnitude of the down slope of the CA output signal is less than or equal to the magnitude of the up slope of the PWM ramp.

CHARGE ALGORITHM

Refer to Figure 3 in UC3906 Data Sheet in the data book.

A) Trickle Charge State
STAT0 = STAT1 = STATLV = logic 0

When CHGNB is less than VREF (2.3V – 3.9mV/°C), STATLV is forced low. This decreases the sense voltage divider ratio, forcing the battery to overcharge (VOC).

$$VOC = (VREF) \bullet \frac{(RS1 + RS2 + RS3 \,||\, RS4)}{(RS3 \,||\, RS4)} \quad (3)$$

During the trickle charge state, the output of the voltage error amplifier is high impedance. The trickle control current is directed into the CA– pin setting the maximum trickle charge current. The trickle charge current is defined in Equation 2.

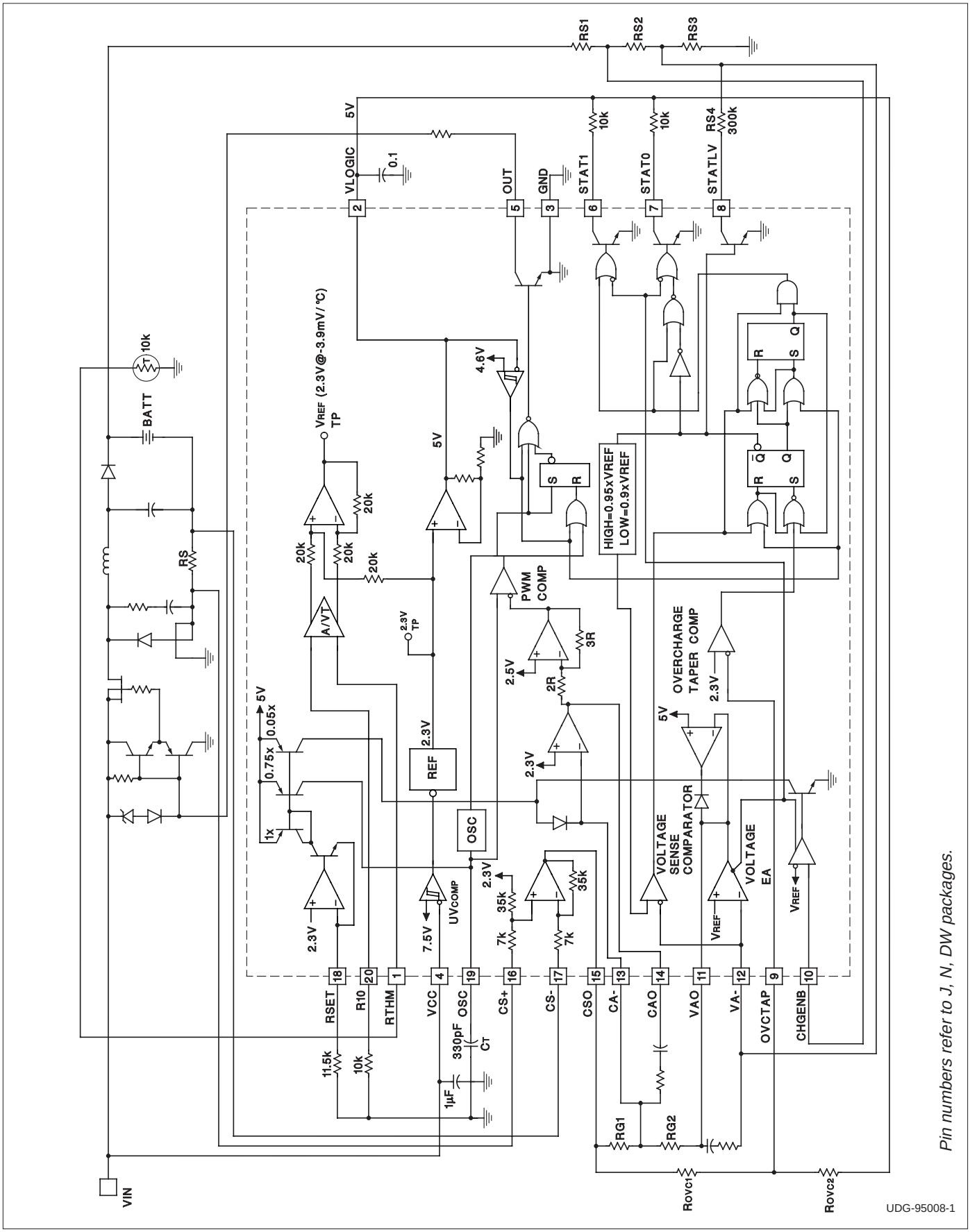
B) Bulk Charge State
STAT1 = STATLV = logic 0, STAT0 = logic 1

As the battery charges, the UC3909 will transition from trickle to bulk charge when CHGENB becomes greater than 2.3V. The transition equation is

$$VT = VREF \bullet \frac{(RS1 + RS2 + RS3 || RS4)}{(RS2 + RS3 || RS4)} \quad (4)$$

STATLV is still driven low.

APPLICATION INFORMATION (cont.)



Pin numbers refer to J, N, DW packages.

Figure 2. Typical application circuit

APPLICATION INFORMATION (cont.)

During the bulk charge state, the voltage error amplifier is now operational and is commanding maximum charge current (I_{BULK}) set by Equation 1. The voltage loop attempts to force the battery to VOC.

C) Overcharge State

STAT0 = STATLV = logic 0, STAT1 = logic 1

The battery voltage surpasses 95% of VOC indicating the UC3909 is in its overcharge state.

During the overcharge charge state, the voltage loop becomes stable and the charge current begins to taper off. As the charge current tapers off, the voltage at CSO increases toward its null point of 2.3V. The center connection of the two resistors between CSO and VLOGIC sets the overcurrent taper threshold (OVCTAP). Knowing the desired overcharge terminate current (I_{OCT}), the resistors R_{OVC1} and R_{OVC2} can be calculated by choosing a value of R_{OVC2} and using the following equation:

$$R_{OVC1} = (18518) \bullet I_{OCT} \bullet RS \bullet R_{OVC2} \quad (5)$$

D) Float State

STAT0 = STAT1 = STATLV = logic 1

The battery charge current tapers below its OVCTAP threshold, and forces STATLV high increasing the voltage sense divider ratio. The voltage loop now forces the battery charger to regulate at its float state voltage (V_F).

$$V_F = (V_{REF}) \frac{(RS1 + RS2 + RS3)}{RS3} \quad (6)$$

If the load drains the battery to less than 90% of V_F, the charger goes back to the bulk charge state, STATE 1.

OFF LINE APPLICATIONS

For off line charge applications, either Figure 3 or Figure 4 can be used as a baseline. Figure 3 has the advantage of high frequency operation resulting in a small isolation transformer. Figure 4 is a simpler design, but at the expense of larger magnetics.

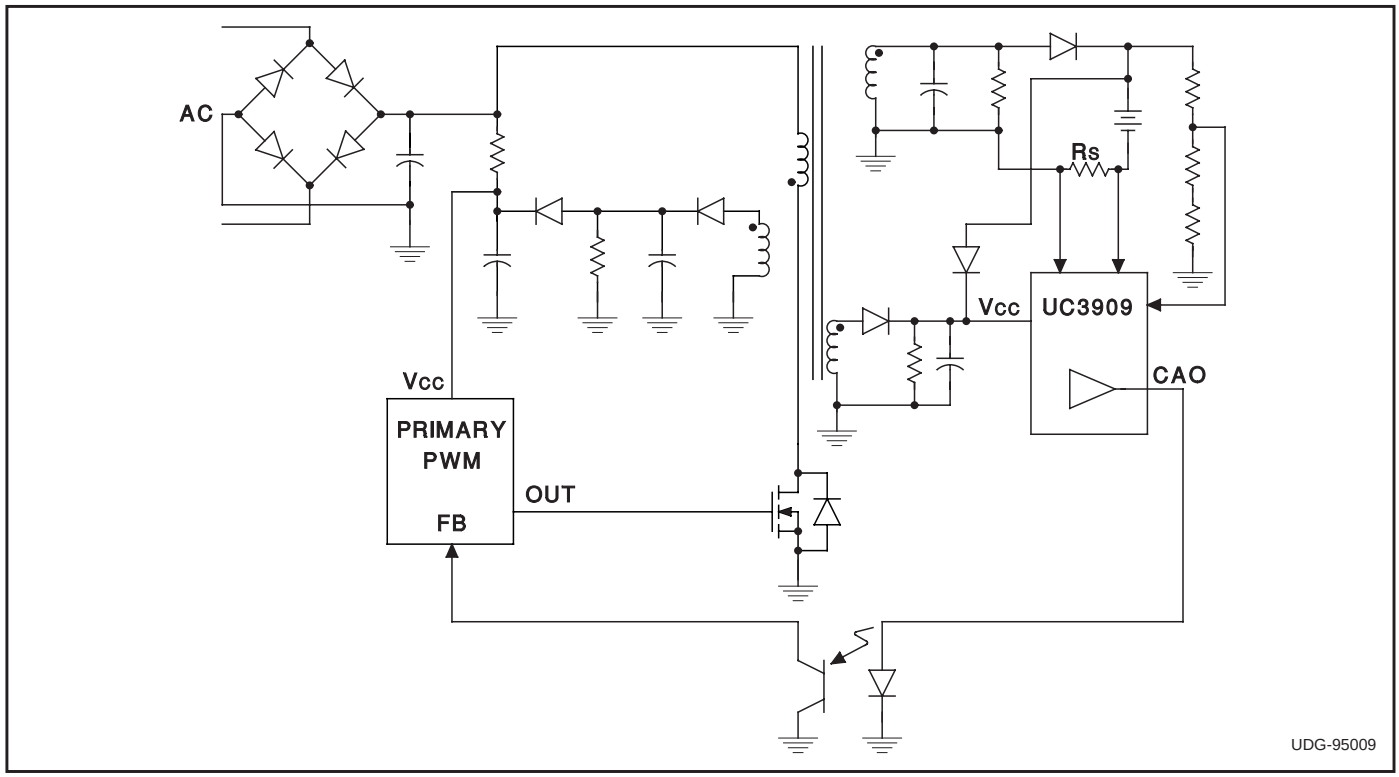


Figure 3. Off line charger with primary side PWM

APPLICATION INFORMATION (cont.)

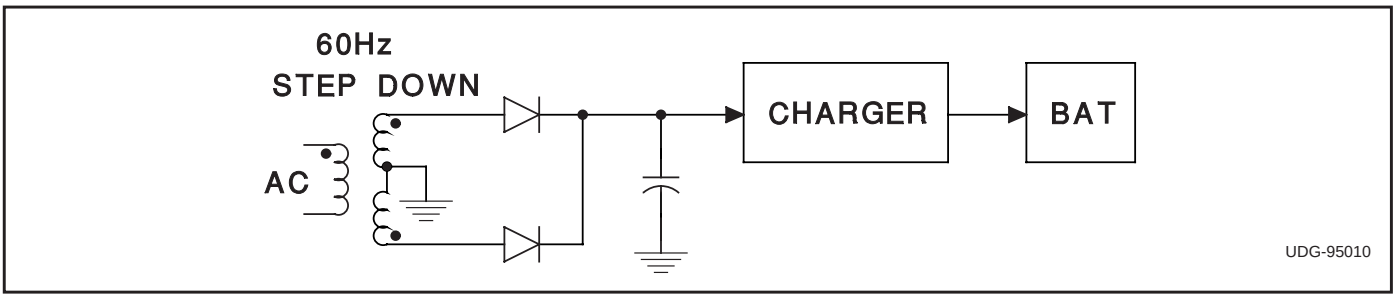


Figure 4. Isolated off line charger

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2909DWTR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	UC2909DW	
UC2909DWTRG4	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UC2909 :

- Enhanced Product: UC2909-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

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